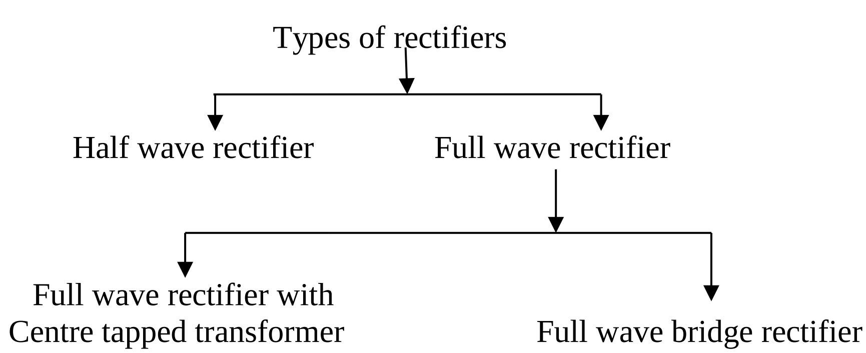
SUMMER – 2022 EXAMINATION

Subject Name: Elements of Electronics **Model Answer :** **22213:EOE**

Important Instructions to examiners:

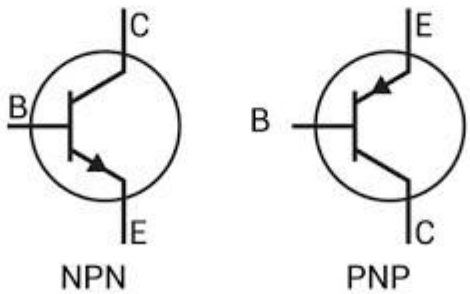
1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answers	Marking Scheme
1		**Attempt any FIVE of the following**	**10 Marks**
1	a)	State the typical knee voltage values for Si and Ge diodes.	
	Ans:	The typical knee voltage values for 1. Si diode = 0.6V 2. Ge diode = 0.2V	 **1 Mark** **1 Mark**
	b)	State the need of rectifiers. List the types of rectifiers.	
	Ans:	Following are the needs of rectifiers:- 1) Every electronics circuit such as amplifiers needs DC power source for its operation, This DC voltage has to be obtained from AC supply. 2) For this the AC supply voltage has to be reduced or stepped down first using a step down transformer and then converted to DC supply by using a rectifier. 3) Thus rectifier is needed to convert AC power source to DC power source	**1 Mark** **1 Mark**



c) Draw a symbol of PNP and NPN transistors.

Ans-



1 Mark each

d) State the output voltage of IC 7824 and IC 7906

Ans : Output voltage of IC 7824 = positive voltage regulator = +24 V **1 Mark**

IC 7906 = negative voltage regulator = - 6 V **1 Mark**

e) Suggest the suitable diode type for voltage regulator circuit

Ans: The suitable diode type for voltage regulator circuit is **Zener diode** **2 Marks**

or

The voltage across zener diode remains constant equal to V_z when it is operated in zener region in reversed biased condition. This fact is utilized in the application of zener diode

f) Define the terms

Ans: **i) Line regulation**

The Line regulation is defined as the change in regulated load voltage due to change in line voltage in specified range of 230 V $\pm$ 10% at a constant load current. **1 Mark**

The Line regulation can be mathematically expressed as **(optional)**

Line regulation = $V_{LH} - V_{LL}$

Where, V_{LH} =Load voltage with high line voltage.

V_{LL} = Load voltage with low line voltage.

ii) Load regulation **1 Mark**

The load regulation (L.R.) is defined as the change in output voltage when the load current is changed from zero (no load) to its maximum (full load) value.

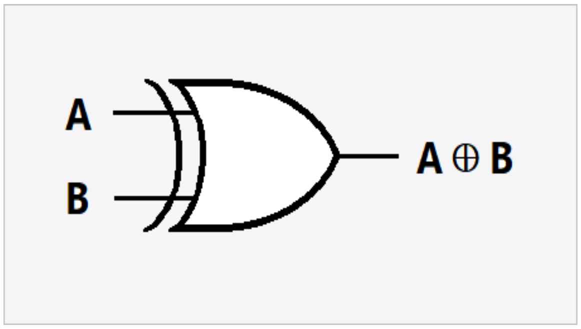
Load regulation = $V_{NL} - V_{FL}$ **(optional)**

where, V_{NL} = Output voltage on no load (zero load current)

V_{FL} = Output voltage on full load (maximum load current).

g) Draw the symbol and truth table of Ex-or gate.

Ans:



Input		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

1 Mark

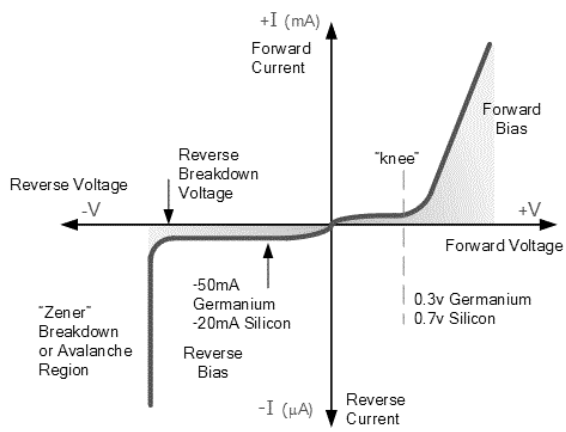
1 Mark

Fig. Truth table of EX OR gate.

2 **Attempt any THREE of following** **12 Marks**

a) Describe the V-I characteristics of a P-N junction diode with proper sketch and define
i) break over voltage
ii) reverse breakdown voltage

Ans: **V-I characteristics of a P-N junction diode:**



2

(1 Mark diagram

1 Mark explanation)

Forward Bias characteristics:

If the external voltage applied on the silicon diode is less than 0.7 volts, the silicon diode allows only a small negligible electric current. When the external voltage applied on the silicon diode reaches 0.7 volts, the p-n junction diode starts allowing large electric current through it. At this point, a small increase in voltage increases the electric current rapidly. The forward voltage at which the silicon diode starts allowing large electric current is called cut-in voltage. The cut-in voltage for silicon diode is approximately 0.7 volts.

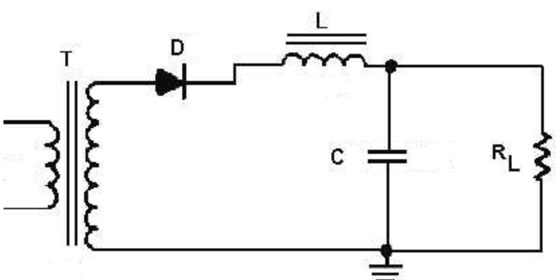
Reverse Bias characteristics:

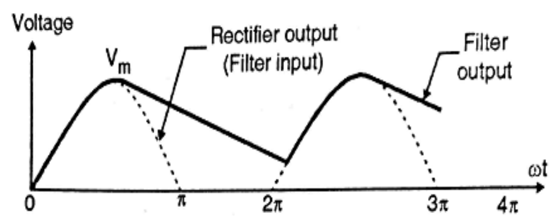
Due to thermal energy in crystal minority carriers are produced. These minority carriers are the electrons and holes pushed towards P-N junction by the negative terminal and positive terminal, respectively. Due to the movement of minority carriers, a very little current flows, which is in nano Ampere range (for silicon). This current is called as reverse saturation current. When the reverse voltage is increased beyond the limit and the reverse current increases drastically is called as reverse breakdown voltage. Diode breakdown occurs by two mechanisms: Avalanche breakdown and Zener breakdown.

1) **Break over voltage-** It is minimum forward voltage at which barrier potential of p-n junction diode breaks and forward diode current starts increasing rapidly. **2 (1 Mark each)**
2) **Reverse breakdown voltage** – It is the reverse voltage at which breakdown of junction take place and large reverse current starts flowing through diode.

b) Describe the working of half wave rectifier with LC filter using neat circuit diagram

Ans:





2 (1 Mark for each figure)

1. The circuit diagram of half wave rectifier with LC filter is combination of inductor in series and capacitor is in shunt with the load resistor.
2. Capacitor input filter is preferred for high values of load resistance and inductor filter is preferred for low values of load resistance.
3. The bleeder resister R_B connected across capacitor is used to maintain continuous current through filter inductance L.
4. In positive half cycle of input AC supply, diode D conducts for complete half positive cycle.
5. The initial voltage on capacitor is assume to be zero and when diode conducts capacitor starts charging through diode up to peak value of secondary input voltage Vm
6. After this secondary input voltage starts reducing and capacitor starts discharging slowly.
7. In negative half cycle capacitor continuous to discharge as diode is reverse biased.
8. Again when positive half cycle begins, diode conducts and capacitor starts charging again up to Vm and cycle repeats.
9. Due to inductor filter in series with the load the current ripple reduces to great extend and load current become smooth.

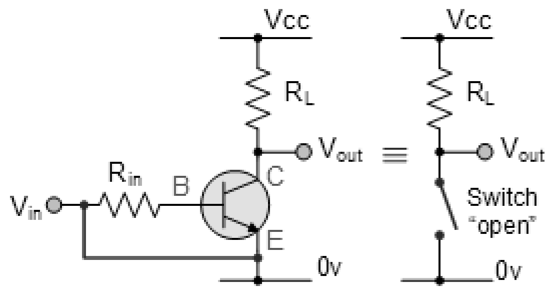
2 Marks for explanation

c) Explain transistor as a switch with neat sketch.

Ans: The transistor can be used as switch, for switching applications it is biased to operate in the saturation (fully on) or cutoff (fully off) regions.

1.Transistor in cutoff region [Open switch]:

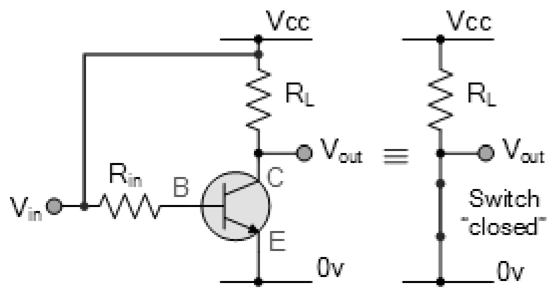
In the cutoff region both the junctions of a transistor are reverse biased and a very small reverse current flows through the transistor. The voltage drop across the transistor (V_{CE}) is high. Thus in the cutoff region the transistor is equivalent to an open switch as shown in Fig.



2 Marks

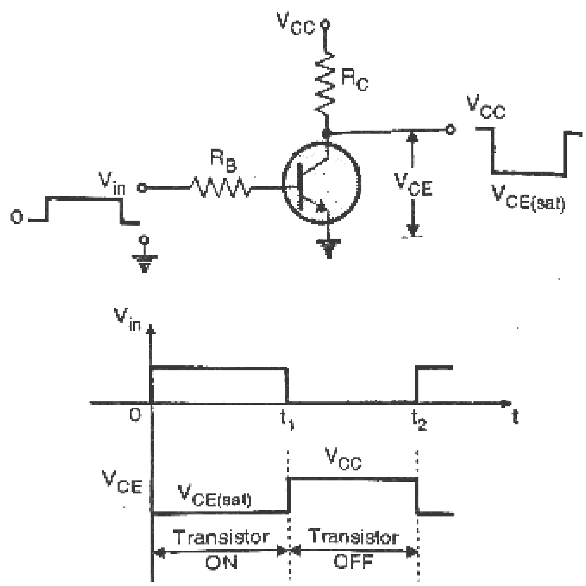
2. Transistor in the saturation region:

When Vin is positive, a large base current flows and the transistor saturates. In the saturation region both the junctions of a transistor are forward biased. The voltage drop across the transistor (V_{CE}) is very small and collector current is very large. In saturation the transistor is equivalent to a closed Switch as shown in Fig.



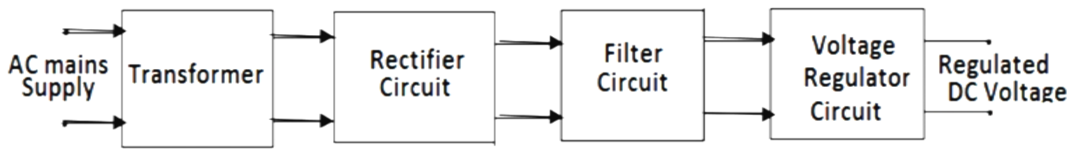
2 Marks

If we apply a square wave at the input of the circuit then the input and output waveform when the transistor acts as a switch are as shown in Fig



d) Sketch the block diagram of DC regulated power supply. State the function of each block.

Ans: **Block Diagram of DC regulated power supply**



2 Marks

The basic building blocks of a regulated dc power supply are

i) A step down transformer
ii) A rectifier
iii) Filter
iv) Voltage regulator

1. The AC mains voltage is applied to a step down transformer. It reduces the amplitude of ac voltage and applies it to a rectifier.
2. The rectifier is usually bridge type full wave rectifier. It converts the AC voltage into a pulsating DC voltage.
3. The ripple in the pulsating dc is reduced by the filter which is connected after the rectifier.
4. The filter can be C type, L type, LC type or CLC type. The output of the filter is a smooth dc voltage with a small ripple.
5. The combination of transformer, rectifier and filter is called as the unregulated power supply.
6. The output of the unregulated power supply is connected at the input of the voltage regulator circuit, to keep the output voltage constant.
7. Thus we get a constant dc voltage at the output of the regulated dc power supply.

2 Marks

3 **Attempt any <u>THREE</u> of the following:** **12 Marks**

a) Explain the functional block diagram of IC 723 with neat sketch

Ans: **Block diagram explanation :**

Temperature compensated zener diode, constant current source and reference amplifier constitutes the reference element. In order to get a fixed voltage from zener diode, the constant current source forces the zener diode to operate at a fixed point.

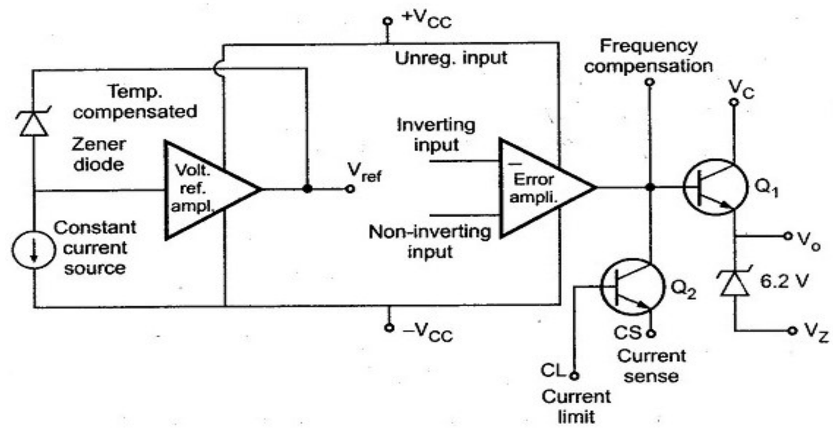
Output voltage is compared with this temperature compensated reference potential of the order of 7 volts. Error amplifier is high gain differential amplifier. It's inverting input is connected to the either whole regulated output voltage or part of that from outside. For later case a potential divider of two scaling resistors is used. Scaling resistors help in getting multiplied reference voltage or scaled up reference voltage.

2 Marks for explanation

Error amplifier controls the series pass transistor Q1, which acts as variable resistor.

The series pass transistor is a small power transistor having about 800 mW dissipation. The unregulated power supply source (< 36 V d.c.) is connected to collector of series pass transistor. Transistor Q2 acts as current limiter in case of short circuit condition. It senses drop across lc placed in series with regulated output voltage externally.

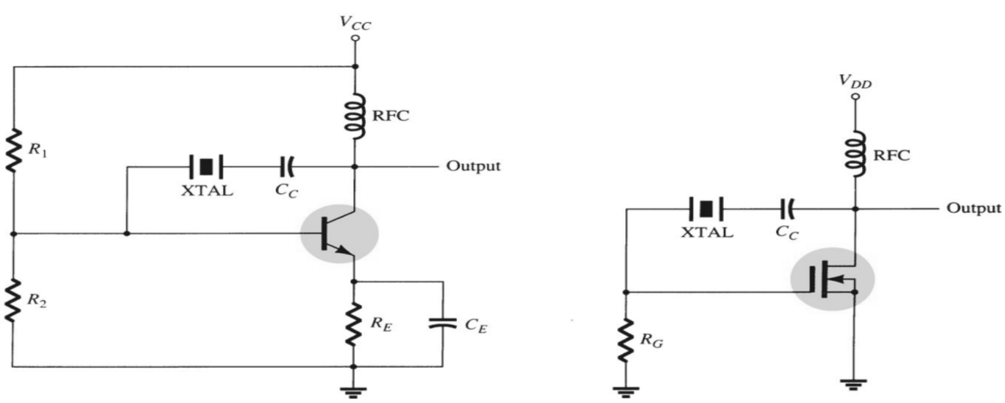
The frequency compensation terminal controls the frequency response of the error amplifier. The required roll-off is obtained by connecting a small capacitor of 100 pF between frequency compensation and inverting input terminals.



2 Marks for circuit diagram

b) Describe the working of crystal oscillator with neat diagram.

Ans:



2 Marks for circuit diagram

Since, in series resonance, crystal impedance is the smallest that causes the crystal provides the largest positive feedback. Resistors R1, R2, and RE provide a voltage-divider stabilized dc bias circuit. Capacitor CE provides ac bypass of the emitter resistor, RE to avoid degeneration. The RFC coil provides dc collector load and also prevents any ac signal from entering the dc supply. The coupling capacitor CC has negligible reactance at circuit operating frequency but blocks any dc flow between collector and base. The oscillation frequency equals the series-resonance frequency of the crystal and is given by:

2 Marks for explanation

$$f_o = \frac{1}{2\pi\sqrt{LC_C}}$$

c) State the various transistor configurations. State any four applications of BJT.

Ans: **Transistor Configurations:**

1. Common Base Configuration (CB)
2. Common Emitter Configuration (CE)
3. Common Collector Configuration (CC)

2 Marks

Applications of BJT :

1. Amplifier
2. Switch
3. Oscillator
4. Random noise generator
5. Pre-amplifier for dynamic microphone
6. Audio mixers
7. Audio modulators

2 Marks for four applications

d) Compare half-wave rectifier with full wave centre-tapped rectifier on the basis of Ripple factor, Rectifier efficiency, TUF and PIV.

Ans:

Sr. No.	**Parameter**	**Half wave rectifier**	**Full wave Centre-taped rectifier**
1	Ripple Factor	1.21	0.482
2	Rectifier Efficiency	40.6%	81.2%
3	TUF	0.286 or 28.6%	0.692 or 69.2%
4	PIV	Vm	2Vm

1 Mark to Each point

4 **Attempt any THREE of the following:** **12 Marks**

a) State the Barkhausen criteria. Draw the circuit diagram of Colpitt's oscillator.

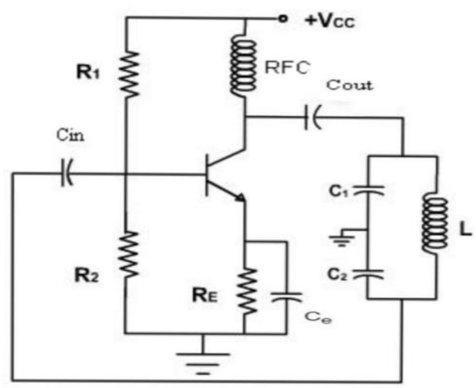
Ans: **Barkhausen's criterion:**

It states that if A is the gain of the amplifying element in the circuit and $\beta(j\omega)$ is the transfer function of the feedback path, so βA is the loop gain around the feedback loop of the circuit, the circuit will sustain steady-state oscillations only at frequencies for which: **2 Marks**

1. The loop gain is equal to unity in absolute magnitude, that is, $|\beta A|=1$ and
2. The phase shift around the loop is zero or an integer multiple of 2π.

Colpitt's Oscillator:

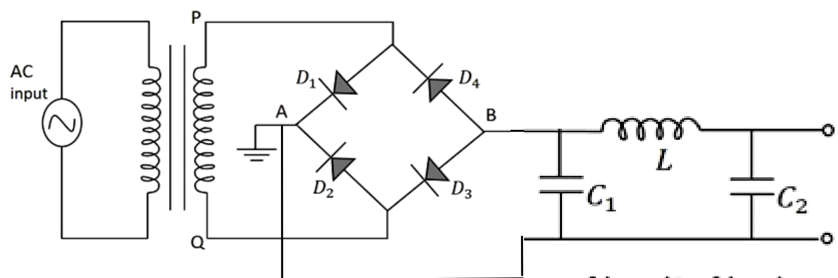
2 Marks



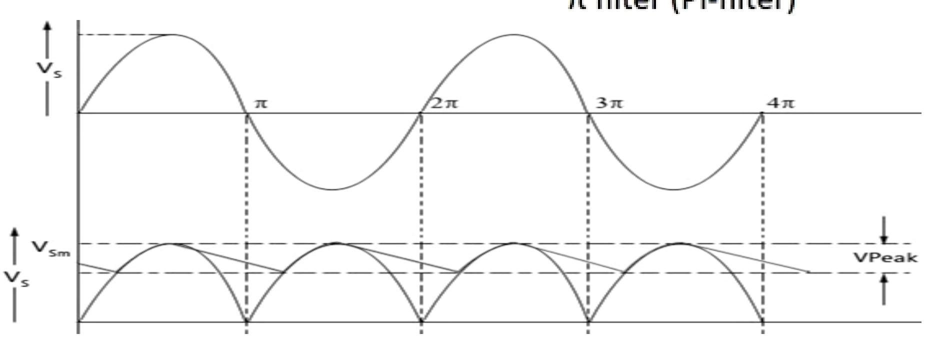
(Or Equivalent diagram)

b) Draw the circuit diagram of bridge rectifier with π filter. Draw it's input and output waveform.

Ans:



2 Marks



2 Marks

c) A transistor has I_B = 110 µA, I_C = 2 mA. Calculate α and β.

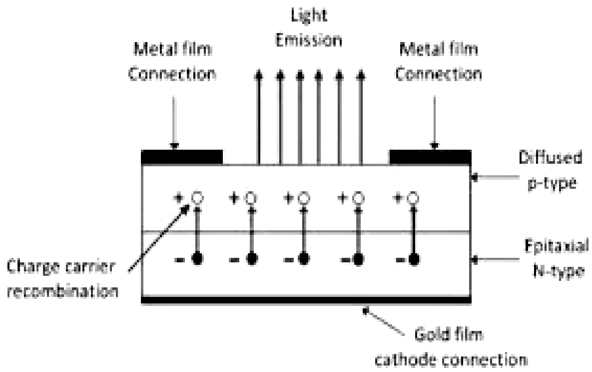
Ans: Given: I_C = 2 mA, I_B = 110 µA

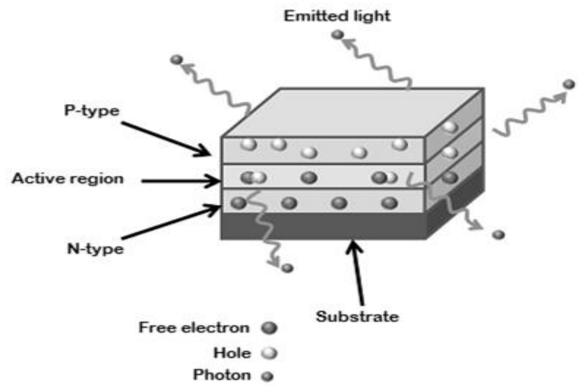
$\beta = I_C / I_B = (2 * 10^{-3}) / (110 * 10^{-6}) = 18.19$ **2 Marks**

$\alpha = \beta/(\beta+1) = 18.19/19.19 = 0.95$ **2 Marks**

d) Describe the construction details of light emitting diode (LED) with neat sketch. State the application of LED.

Ans:





2 Marks

(Any one of the above or other equivalent figure)

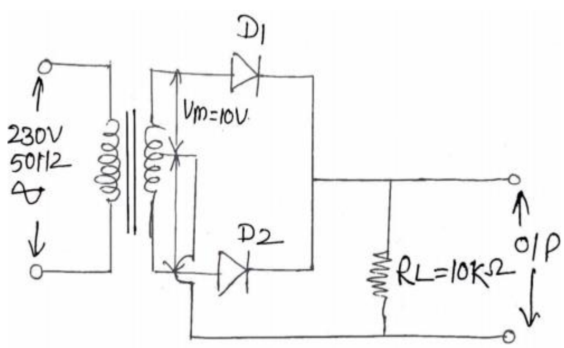
One of the methods used to construct LED is to deposit three semiconductor layers on the substrate. The three semiconductor layers deposited on the substrate are n-type semiconductor, p-type semiconductor and active region. Active region is present in between the n-type and p-type semiconductor layers. Most of the charge carriers recombine at active region. Therefore, most of the light is emitted by the active region. The active region is also called as depletion region. **1 Mark**

Applications of LED:

1. TV Backlighting.
1. Smartphone Backlighting.
2. LED displays.
3. Automotive Lighting
4. Dimming of lights.

1 Mark (any 2 applications)

e) Figure No. 0 l. shows the centre tapped full wave rectifier circuit. Assume both the diodes to be ideal. Determine : i) DC output voltage (V_{dc}) and ii) Peak inverse voltage (PIV) of diode



Ans: Given: Vm = 10V

$V_{dc} = 2Vm / \pi = 20/3.14 = 6.37$ **V** **2 Marks**

PIV = 2Vm = 20 **V** **2 Marks**

5 **Attempt any TWO of the following:** **12 Marks**

a) A transistor has a typical β=100. If the collector current is 40 mA. Determine the value of base current, emitter current and α. **6 Marks**

Ans: Given: β=100, Ic = 40 mA

As $I_C = \beta . I_B$ **2 Marks for Base current**

∴ $I_B = I_C / \beta$

∴ $I_B = 0.4$ mA

Therefore, base current is 0.4 mA.

Now, $I_E = I_C + I_B$ ………….(Assume $I_{CBO} = 0$) **2 Marks for emitter current**

∴ $I_E = 44$ mA

Therefore, emitter current is 44 mA.

As $\alpha = I_C / I_E$

∴ $\alpha = 0.909$ **2 Marks for α**

b) For Zener voltage regulator, if I_{Zmin} = 2 mA, I_{Zmax} = 20 mA, V_Z= 4.7 V. Determine the range of input voltage over which output voltage remains constant. R_L= 1 KΩ, R= 1 Ω, Z_Z= 0 Ω. Refer Figure No. 02. **6 Marks**

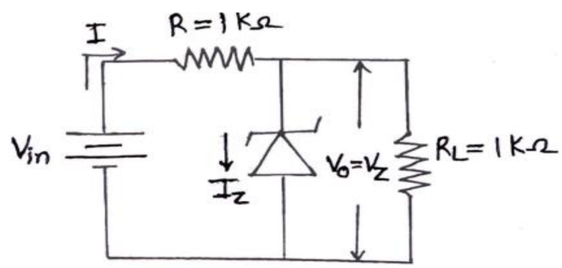


Figure No. 02.

Ans: Given R= 1 KΩ, R_L= 1 KΩ, $I_{zmin} = 2\,mA$, $I_{zmax} = 20\,mA$

V_z= 4.7 V

So $V_o = V_z$= 4.7 V

The input voltage range:

i) $V_{in.max} = I_{Rmax} \times R + V_Z$ ……………(1)

But $I_{Rmax} = I_{zmax} + I_L$

$= I_{zmax} + V_Z/R_L$

$\therefore I_{Rmax} = 24.7$ mA **3 Marks for stepwise solution of Vin.max**

Therefore from (1), We have

$V_{in.max} = 29.4$ V

ii) $V_{in.min} = I \times R + V_Z$ **3 Marks for stepwise solution of Vin.min**

But $I = I_{zmin} + I_L$

$\therefore$ I = 6.7 mA

$\therefore V_{in.min} = 11.4$ V

So, input voltage ranging from 11.4 V to 29.4 V.

c) State the disadvantage of JK flip-flop. Explain the working of MS .JK flip-flop with proper diagram. **6 Marks**

Ans: JK Flip-Flop has a disadvantage of timing problem which is known as "Race-around ". i.e. the output Q changes its state between 0 &1 before the timing pulse of the clock input goes to the OFF state. **2Marks for State**

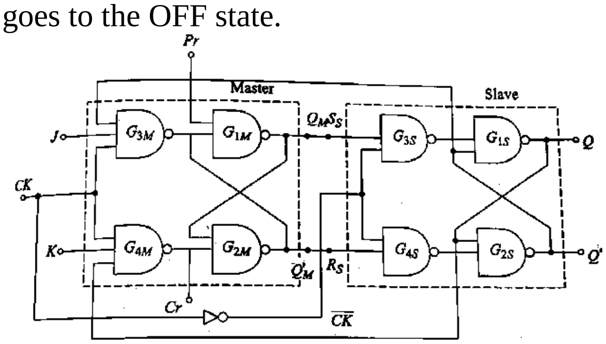


Fig. Master-Slave J-K Flip-Flop

J	K	Q	Q'
0	0	Q	Q'
0	1	0	1
1	0	1	0
1	1	Q'	Q

Fig. Truth Table of J-K Flip-Flop

2 Marks for Diagram

A "MS J-K flip-flop" is a combination of 2 S-R flip-flops (i.e. MASTER and SLAVE) with feedback from the outputs of the second flip-flop to the inputs of first flip-flop. Positive clock pulses are applied to the first flip-flop and the inverted clock pulses are applied to the second flip-flop. **2 Marks for Working**

Working:

When J = 0, K = 0, there will be no change in the output with or without clock pulse. When J = 1, K = 0, and clock pulse is on positive edge, the output of master flip flop Q is set as high, and when the negative edge of the clock arrives, the output of master flip flop passes through the slave flip flop and produce output. When J = 0, K = 1, and clock pulse is on positive edge, the output of master flip flop Q is set as low and Q' is set as high, when the negative clock edge arrives the Q output of the master flip flop feed into the slave flip flop, and that causes to set the output of the slave Q as low. When J = K = 1, then at the positive edge of the clock pulse, the master flip flop toggles (means the change of the previous state into its opposite state), and at the negative edge of the clock pulse, the slave flip flop toggles.

6 **Attempt any TWO of the following.** **12 Marks**

a) Compare RC and LC oscillators. (six points)

Ans:

S. N.	RC Oscillator	LC Oscillator
1	Uses Transistors & Resistance-Capacitance circuits	Uses Transistors & LC tuned circuits.
2	Frequency of oscillations is dependent on the values of R & C.	Frequency of oscillations is dependent on the values of R & L.
3	It is used at low & Medium frequency.	It is used at High Frequency.
4	It has poor frequency stability.	It has poor frequency stability except for the clapp Oscillator
5	E.g. Phase Shift Oscillator, Wein Bridge Oscillator	E.g. Hartley Oscillator, Colpitt's Oscillator & Clapp Oscillator
6	It is used at low & Medium Frequency signal generator.	It is used in Radios, TV as Frequency synthesizer.

1 Mark for Each point

b) Sketch common base configuration input characteristics for two different values of VCB and 0/P characteristics for two different values IE. Write the formula for input resistance and output resistance.

Ans:

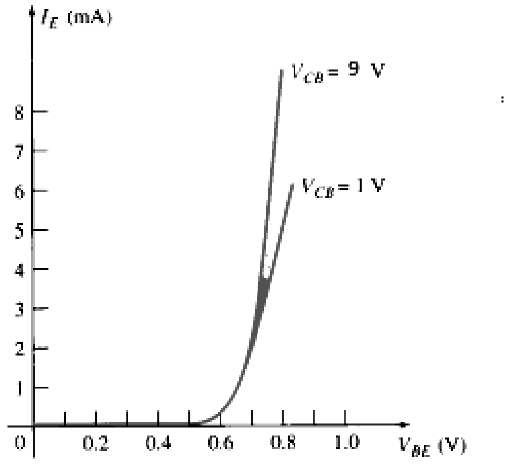


Fig. Input Characteristics of NPN Transistor for CB Configuration

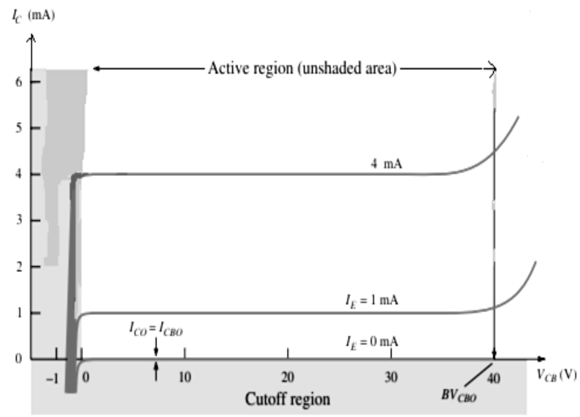


Fig. Output Characteristics of NPN Transistor For CB Configuration

(Input characteristics- 2 Marks & Output characteristics- 2 Marks)

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}, \qquad V_{CB} = \text{constant}$$ **(1 Mark)**

$$r_O = \frac{\Delta V_{CB}}{\Delta I_C}, \qquad I_E = \text{constant}$$ **(1 Mark)**

c) Convert the following
i) $(208)_{10} = (\quad)_2$
ii) $(A9C)_{16} = (\quad)_8$
iii) $(247)_8 = (\quad)_{10}$

6 Marks

Ans: i)

2	208	0
2	104	0
2	52	0
2	26	0
2	13	1
2	6	0
2	3	1
2	1	1

$\therefore \mathbf{(208)_{10} = (11010000)_2}$

1 Mark for steps and

1 Mark for correct answer

(for each bit)

ii) $(A9C)_{16} = (1010\ \ 1001\ \ 1100)_2$

$= (101\ \ 010\ \ 011\ \ 100)_2$
$= (\ 5\quad 2\quad 3\quad 4\ )_8$
$\therefore \boldsymbol{(A9C)_{16} = (5234)_8}$

iii) $(247)_8 = 2\times8^2 + 4\times8^1 + 7\times8^0$
$= 128+32+07$
$\therefore \mathbf{(247)_8 = (167)_{10}}$